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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,627	HONG, SUNGKWON C.	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26 and 27* is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/03, 10/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on July 15, 2003.

Fig. 6, a cross-sectional view of Fig. 5's plan view, is objected to because it is inconsistent with Fig. 5. Specifically, Fig. 5's plan view correctly illustrates floating diffusion node 25 extending underneath capacitor 82, but Fig. 6's cross-sectional view does not illustrate floating diffusion node 25 extending underneath capacitor 82. Correction is required (i.e., Fig. 6 should be corrected to show floating diffusion node 25 extending underneath capacitor 82, consistent with Fig. 5's plan view).

Claims 1, 6 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori (United States Patent 5,422,669, cited in the Information Disclosure Statement filed on October 29, 2004).

With respect to independent claim 1, Mori discloses a method of operating an imager (see the entire reference, including the Figs. 1-4 disclosure), comprising: generating charges with a photosensor 14, transferring charges from said photosensor to a storage node (i.e., the node in the middle of Fig. 2's element 24); selectively increasing the charge storage capacity of said node (via capacitance elements 35-37); and producing an electrical signal in response to charges transferred to said node.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Mori.

With respect to dependent claim 6, Mori's imager is a CCD imager.

Claim 6 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Mori.

With respect to independent claim 17, Mori discloses a pixel of an imager (see the entire reference, including the Figs. 1-4 disclosure), said pixel comprising: a photosensing region 14 which receives incident light and generates photoelectric

charges; a diffusion region for receiving photogenerated charges from said photosensing region (i.e., the node in the middle of Fig. 2's element 24); and at least one capacitor 35 switchably operable to increase capacitance of said diffusion region.

Claim 17 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Mori.

Claims 1-5 and 7-25 are rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann (European Patent Application EP 1 231 641, cited in the Information Disclosure Statement filed on October 29, 2004).

With respect to independent claim 1, Lauxtermann discloses a method of operating an imager (see the entire reference, including the Fig. 4 disclosure, for example), comprising: generating charges with a photosensor, transferring charges from said photosensor to a storage node; selectively increasing the charge storage capacity of said node (via the switchable MOS gate capacitor CM); and producing an electrical signal in response to charges transferred to said node.

Claim 1 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 2, Lauxtermann's act of selectively increasing the charge storage capacity of said node comprises selectively activating a gate capacitor CM coupled to said node.

Claim 2 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 3, activating Lauxtermann's gate capacitor CM operates to eliminate substantially all charge in the photosensor during said transfer.

Claim 3 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 4, Lauxtermann's act of selectively increasing the charge storage capacity of said node occurs prior to said charge transfer.

Claim 4 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 5, Lauxtermann's imager is a CMOS imager.

Claim 5 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 7, Lauxtermann discloses an integrated circuit (see the entire reference, including the Figs. 4-8 disclosure, for example), comprising: a substrate; and a pixel array, each pixel in the pixel array comprising: a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region for receiving the photoelectric charge; and at least one gate capacitor CM connected to the floating diffusion region, each gate capacitor operable to increase a charge storage capacitance of the floating diffusion region.

Claim 7 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 8, Lauxtermann's photosensor is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 8 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 9, Lauxtermann's at least one gate capacitor CM comprises a lower capacitor plate electrically coupled to the floating diffusion region and an upper capacitor plate connected to a contact.

Claim 9 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 10, Lauxtermann's at least one gate capacitor CM is located between a transfer gate SH and a reset gate RS.

Claim 10 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 11, Lauxtermann's at least one gate capacitor CM is formed over a portion of the floating diffusion region (see Fig. 8, for example).

Claim 11 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 12, Lauxtermann's pixel array is a CMOS pixel array.

Claim 12 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 13, Lauxtermann's pixel array is operated by timing and control circuitry.

Claim 13 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 14, Lauxtermann's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor CM.

Claim 14 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 15, Lauxtermann discloses a method of forming a pixel (see the entire reference, including the Figs. 4-8 disclosure, for example), comprising: forming a photosensor on a substrate, said photosensor detecting and storing photon energy; forming a transfer gate SH on said substrate; forming a floating diffusion region on said substrate; and forming a gate capacitor CM over said substrate, the gate capacitor being connected to the floating diffusion region.

Claim 15 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 16, Lauxtermann's gate capacitor CM is formed over a portion of the floating diffusion region (see Fig. 8, for example).

Claim 16 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 17, Lauxtermann discloses a pixel of an imager (see the entire reference, including the Figs. 4-8 disclosure, for example), said pixel comprising: a photosensing region which receives incident light and generates photoelectric charges; a diffusion region for receiving photogenerated charges from said photosensing region; and at least one capacitor CM switchably operable to increase capacitance of said diffusion region.

Claim 17 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 18, Lauxtermann's capacitor CM is a gate capacitor.

Claim 18 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 19, Lauxtermann discloses a method of achieving high conversion gain in an image sensor (see the entire reference, including the Figs. 4-8 disclosure, for example), said method comprising: activating at least one photosensor at or beneath a surface of a substrate, wherein each photosensor operates to detect photon energy and convert said photon energy to photoelectric charge; activating a gate capacitor CM to increase charge storing capacitance of a storage node; transferring said photoelectric charge generated in each photosensor to said storage node; and converting said photoelectric charge at said storage node to an electrical signal.

Claim 19 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 20, Lauxtermann discloses an image pixel array in an imaging device (see the entire reference, including the Figs. 4-8 disclosure, for example), each pixel in the pixel array comprising: a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region for receiving the photoelectric charge; and at least one gate capacitor

CM connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 20 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 21, Lauxtermann's photosensor is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 21 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to independent claim 22, Lauxtermann discloses a CMOS image system (see the entire reference, including the Figs. 4-8 disclosure, for example), comprising: a processor; and an imaging device coupled to said processor, said imaging device comprising: a pixel array, each pixel in the pixel array comprising: a photosensor operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region for receiving the photoelectric charge; and at least one gate capacitor CM connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 22 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 23, Lauxtermann's CMOS imager system further comprises timing and control circuitry for operation of the pixel array.

Claim 23 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 24, Lauxtermann's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor CM.

Claim 24 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

With respect to dependent claim 25, Lauxtermann's at least one gate capacitor CM increases total charge capacitance such that said imager system has increased responsiveness to low light and high light signal conditions.

Claim 25 is thus rejected under 35 U.S.C. 102(a) as being anticipated by Lauxtermann.

Claims 1-5, 7-9 and 11-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill et al. (United States Patent 6,512,544 – hereafter Merrill - cited in the Information Disclosure Statement filed on October 29, 2004).

With respect to independent claim 1, Merrill discloses a method of operating an imager (see the entire reference, including the Fig. 6 disclosure, for example), comprising: generating charges with a photosensor 122, transferring charges from said photosensor to a storage node (at V_{DIFF}); selectively increasing the charge storage capacity of said node (via capacitor 132); and producing an electrical signal in response to charges transferred to said node.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 2, Merrill's act of selectively increasing the charge storage capacity of said node comprises selectively activating a gate capacitor 132 coupled to said node.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 3, activating Merrill's gate capacitor 132 operates to eliminate substantially all charge in the photosensor during said transfer.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 4, Merrill's act of selectively increasing the charge storage capacity of said node occurs prior to said charge transfer.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 5, Merrill's imager is a CMOS imager.

Claim 5 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 7, Merrill discloses an integrated circuit (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), comprising: a substrate 270; and a pixel array, each pixel in the pixel array comprising: a photosensor 122 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 274 for receiving the photoelectric charge; and at least one gate capacitor 132 connected to the floating diffusion region, each gate capacitor operable to increase a charge storage capacitance of the floating diffusion region.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 8, Merrill's photosensor is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 9, Merrill's at least one gate capacitor 132 comprises a lower capacitor plate 138 electrically coupled to the floating diffusion region and an upper capacitor plate 140 connected to a contact.

Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 11, Merrill's at least one gate capacitor 132 is formed over a portion of the floating diffusion region 274.

Claim 11 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 12, Merrill's pixel array is a CMOS pixel array.

Claim 12 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 13, Merrill's pixel array is operated by timing and control circuitry.

Claim 13 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 14, Merrill's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor 132.

Claim 14 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 15, Merrill discloses a method of forming a pixel (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), comprising: forming a photosensor 122 on a substrate 270, said photosensor detecting and storing photon energy; forming a transfer gate 134 on said substrate; forming a

floating diffusion region 274 on said substrate; and forming a gate capacitor 132 over said substrate, the gate capacitor being connected to the floating diffusion region.

Claim 15 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 16, Merrill's gate capacitor 132 is formed over a portion of the floating diffusion region 274.

Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 17, Merrill discloses a pixel of an imager (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), said pixel comprising: a photosensing region 122 which receives incident light and generates photoelectric charges; a diffusion region 274 for receiving photogenerated charges from said photosensing region; and at least one capacitor 132 switchably operable to increase capacitance of said diffusion region.

Claim 17 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 18, Merrill's capacitor 132 is a gate capacitor.

Claim 18 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 19, Merrill discloses a method of achieving high conversion gain in an image sensor (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), said method comprising: activating at least one photosensor 122 at or beneath a surface of a substrate 270, wherein each photosensor operates to detect photon energy and convert said photon energy to photoelectric charge; activating a gate capacitor 132 to increase charge storing capacitance of a storage node (the node at V_{DIFF} in Fig. 8); transferring said photoelectric charge

generated in each photosensor to said storage node; and converting said photoelectric charge at said storage node to an electrical signal.

Claim 19 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 20, Merrill discloses an image pixel array in an imaging device (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), each pixel in the pixel array comprising: a photosensor 122 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 274 for receiving the photoelectric charge; and at least one gate capacitor 132 connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 20 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 21, Merrill's photosensor 122 is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 21 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to independent claim 22, Merrill discloses a CMOS image system (see the entire reference, including the Fig. 6 and Fig. 12 disclosure, for example), comprising: a processor; and an imaging device coupled to said processor, said imaging device comprising: a pixel array, each pixel in the pixel array comprising: a photosensor 122 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 274 for receiving the photoelectric charge; and at least one gate capacitor 132 connected to the floating diffusion region,

each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 22 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 23, Merrill's CMOS imager system further comprises timing and control circuitry for operation of the pixel array.

Claim 23 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 24, Merrill's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor 132.

Claim 24 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

With respect to dependent claim 25, Merrill's at least one gate capacitor 132 increases total charge capacitance such that said imager system has increased responsiveness to low light and high light signal conditions.

Claim 25 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Merrill.

Claims 1-5, 7-9, 11-14 and 17-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (United States Patent 6,246,436 – hereafter Lin - cited in the Information Disclosure Statement filed on October 29, 2004).

With respect to independent claim 1, Lin discloses a method of operating an imager (see the entire reference, including the Fig. 3 disclosure, for example), comprising: generating charges with a photosensor D2, transferring charges from said photosensor to a storage node N1; selectively increasing the charge storage capacity of said node (via gate capacitor GC); and producing an electrical signal in response to charges transferred to said node.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 2, Lin's act of selectively increasing the charge storage capacity of said node comprises selectively activating a gate capacitor GC coupled to said node N1.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 3, activating Lin's gate capacitor GC operates to eliminate substantially all charge in the photosensor during said transfer.

Claim 3 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 4, Lin's act of selectively increasing the charge storage capacity of said node occurs prior to said charge transfer.

Claim 4 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 5, Lin's imager is a CMOS imager.

Claim 5 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to independent claim 7, Lin discloses an integrated circuit (see the entire reference, including the Figs. 3-6 disclosure, for example), comprising: a substrate 610; and a pixel array, each pixel in the pixel array comprising: a photosensor D2 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 612/610 for receiving the photoelectric charge; and at least one gate capacitor GC connected to the floating diffusion region, each gate capacitor operable to increase a charge storage capacitance of the floating diffusion region.

Claim 7 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 8, Lin's photosensor is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 8 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 9, Lin's at least one gate capacitor GC comprises a lower capacitor plate electrically coupled to the floating diffusion region 612/610 and an upper capacitor plate 630 connected to a contact.

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 11, Lin's at least one gate capacitor GC is formed over a portion of the floating diffusion region 612/610.

Claim 11 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 12, Lin's pixel array is a CMOS pixel array.

Claim 12 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 13, Lin's pixel array is operated by timing and control circuitry.

Claim 13 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin's.

With respect to dependent claim 14, Lin's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor GC.

Claim 14 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to independent claim 17, Lin discloses a pixel of an imager (see the entire reference, including the Figs. 3-6 disclosure, for example), said pixel comprising: a photosensing region D2 which receives incident light and generates photoelectric charges; a diffusion region 612/610 for receiving photogenerated charges from said

photosensing region; and at least one capacitor GC switchably operable to increase capacitance of said diffusion region.

Claim 17 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 18, Lin's capacitor GC is a gate capacitor.

Claim 18 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to independent claim 19, Lin discloses a method of achieving high conversion gain in an image sensor (see the entire reference, including the Figs. 3-6 disclosure, for example), said method comprising: activating at least one photosensor D2 at or beneath a surface of a substrate 610, wherein each photosensor operates to detect photon energy and convert said photon energy to photoelectric charge; activating a gate capacitor GC to increase charge storing capacitance of a storage node N1; transferring said photoelectric charge generated in each photosensor to said storage node; and converting said photoelectric charge at said storage node to an electrical signal.

Claim 19 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to independent claim 20, Lin discloses an image pixel array in an imaging device (see the entire reference, including the Figs. 3-6 disclosure, for example), each pixel in the pixel array comprising: a photosensor D2 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 612/610 for receiving the photoelectric charge; and at least one gate capacitor GC connected to the floating diffusion region, each gate capacitor being

selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 20 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 21, Lin's photosensor D2 is selected from the group consisting of a photodiode, photogate, and a photoconductor.

Claim 21 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to independent claim 22, Lin discloses a CMOS image system (see the entire reference, including the Figs. 3-6 disclosure, for example), comprising: a processor; and an imaging device coupled to said processor, said imaging device comprising: a pixel array, each pixel in the pixel array comprising: a photosensor D2 operable to receive photon energy and convert the photon energy to photoelectric charge; a floating diffusion region 612/610 for receiving the photoelectric charge; and at least one gate capacitor GC connected to the floating diffusion region, each gate capacitor being selectively operable to increase a charge storage capacitance of the floating diffusion region.

Claim 22 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 23, Lin's CMOS imager system further comprises timing and control circuitry for operation of the pixel array.

Claim 23 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 24, Lin's timing and control circuitry generates a timing signal to selectively operate the at least one gate capacitor GC.

Claim 24 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

With respect to dependent claim 25, Lin's at least one gate capacitor GC increases total charge capacitance such that said imager system has increased responsiveness to low light and high light signal conditions.

Claim 25 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

Claims 26 and 27 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable CCD imagers taken as a whole, including the gate capacitor.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner